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1 Pseudo-random testing and signature analysis for mixed-signal circuits

Chen-Yang Pan, Kwang-Ting Cheng

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(88.30 KB) Additional Information: full citation, abstract, references, index terms

Publisher Site

In this paper, we address the problem of functional testing of mixed-signal circuits using pseudo-random patterns. By embedding the linear, time-invariant (LTI) analog circuit between a digital-to-analog converter (DAC) and an analog-to-digital converter (ADC), we can model the analog and converter circuitry as a digital LTI system and test it using the pseudo-random vectors. We give mathematical analysis and formulate the pseudo-random testing process as the linear transformation of a random pr ...

Keywords: Pseudo-Random Testing, Random Process, Signature Analysis, Impulse Response

2 Efficient and accurate testing of analog-to-digital converters using oscillation-test method

K. Arabi, B. Kaminska

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Full text available: pdf(511.01 KB) Additional Information: full citation, abstract

Publisher Site

This paper describes a practical test approach for analog-to-digital converters (ADCs) based on the oscillation-test strategy. The oscillation-test is applied to convert the ADC under test to an oscillator. The oscillation frequencies are able to monitor the ADC conversion rate, differential nonlinearity (DNL) and integral nonlinearity (INL) at each quantization band edge (QBE). Using this method, no analog stimulus should be supplied and therefore the need for a costly precision signal generato ...

Keywords: A/D convertor, ADC conversion rate, ADC testing, analog-to-digital converters, analogue-digital conversion, differential nonlinearity, digital circuitry, integral nonlinearity, oscillation-test method, quantization band edge

3 Implementation of a linear histogram BIST for ADCs
F. Azaïs, S. Bernard, Y. Bertrand, M. Renovell
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(476.52 KB) Additional Information: full citation, references, index terms

4 A strategy for real-time kernel support in application-specific HW/SW embedded architectures
Steven Vercauteren, Bill Lin, Hugo De Man
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(91.67 KB) Additional Information: full citation, references, citings, index terms

5 Energy-aware system design: A low-energy chip-set for wireless intercom
M. Josie Ammer, Michael Sheets, Tufan Karalar, Mika Kuulusa, Jan Rabaey
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(510.83 KB) Additional Information: full citation, abstract, references, index terms

A low power wireless intercom system is designed and implemented. Two fully-operational ASICs, integrating custom and commercial IP, implement the entire digital portion of the protocol stack. Combined, the chips consume 13 mW on average when three nodes are connected to the network. A high-level design methodology was used to define the protocol stack and communication algorithms, select architectures, and minimize energy.

Keywords: design methodology, low power, wireless communication

6 A New Design Flow and Testability Measure for the Generation of a Structural Test and BIST for Analogue and Mixed-Signal Circuits
C. Hoffmann
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(339.35 KB) Publisher Site Additional Information: full citation, abstract

For the generation of defect-oriented tests a system is de-velopedthat includes the synthesis of self-test structures.With the objective to generate a highly efficient analoguetest, the fault simulation methods are greatly enhanced: (1)A new testability measure, (2)the possibility to distinguishbetween not-to-detect and hard-to-detect faults with respectto the tolerances of the respective measurement system. Bypresenting a new design flow and using the fault simulationin a very early design stag ...

7 TAM Optimization for Mixed-Signal SOCs using Analog Test Wrappers
Anuja Sehgal, Sule Ozev, Krishnendu Chakrabarty
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(167.79 KB) Additional Information: full citation, abstract, citings, index terms

We present a new approach for TAM optimization and testscheduling in the modular testing of mixed-signal SOCs. A testplanning approach for digital SOCs is extended to handle analogcores in a plug-and-play fashion. A test wrapper based on anADC/DAC pair and a digital configuration circuit is designed foranalog cores such that these cores can be accessed through digitalTAMs. In this way, there is no dependence on an analog testbus and expensive mixed-signal testers. Experimental results arepresent ...

8 A case study of synthesis for industrial-scale analog IP: redesign of the equalizer/filter frontend for an ADSL CODEC

Rodney Phelps, Michael J. Krasnicki, Rob A. Rutenbar, L. Richard Carley, James R. Hellums
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(211.88 KB) Additional Information: full citation, abstract, references, citings, index terms

A persistent criticism of analog synthesis techniques is that they cannot cope with the complexity of realistic industrial designs, especially system-level designs. We show how recent advances in simulation-based synthesis can be augmented, via appropriate macromodeling, to attack complex analog blocks. To support this claim, we resynthesize from scratch, in several different styles, a complex equalizer/filter block from the frontend of a commercial ADSL CODEC, and verify by full si ...

9 Analog design for reuse - case study: very low-voltage sigma-delta modulator

M. Dessouky, A. Kaiser, M. Louërat, A. Greiner
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(360.20 KB) Additional Information: full citation, references, index terms

10 Session 5B: Embedded tutorial: CAD solutions and outstanding challenges for mixed-signal and RF IC design: CAD solutions and outstanding challenges for mixed-signal and RFIC design

Domine Leenaerts, Georges Gielen, Rob A. Rutenbar
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(1.87 MB) Additional Information: full citation, abstract, references, index terms

This tutorial paper addresses the problems and solutions that are posed by the design of mixed-signal integrated systems on chip (SoC). These include problems in mixed-signal design methodologies and flows, problems in analog design productivity, as well as open problems in analog, mixed-signal and RF design, modeling and verification tools. The tutorial explains the problems that are posed by these mixed-signal/RF SoC designs, describes the solutions and their underlying methods that exist toda ...

11 (Special session) presentation + poster disscussion: university design contest: A dual-band switching digital controller for a buck converter

Martin Yeung-Kei Chui, Wing-Hung Ki, Chi-Ying Tsui
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**

Full text available: pdf(264.69 KB) Additional Information: full citation, abstract, references

A 0.6μm CMOS integrated digital PID controller for a buck converter is fabricated and tested. It consists of: (1) a VCO driving a counter to serve as an ADC; (2) a PID compensator that employs a programmable integration time for enhancing accuracy and stability; and (3) a dual-band switching PWM generator with a modified tapped delay line for better output resolution and area efficiency. The converter switches at 1 MHz, while the tracking time is 50μs for a step change of IV.

12 Pandora - an experimental system for multimedia applications

Andy Hopper
April 1990 **ACM SIGOPS Operating Systems Review**, Volume 24 Issue 2

Full text available: pdf(1.43 MB) Additional Information: full citation, abstract, citings

Pandora is a joint project between Olivetti Research Cambridge and the University of Cambridge Computer Laboratory. The project is investigating the use of multimedia workstations in a working environment with particular emphasis on digital video. It endeavours to place a camera on the desktop to make generation of multimedia documents as easy as producing text. We are aiming to produce a number of new applications as well as to provide insights into the way computer systems should be designed.T ...

13 Synchroscalar: A Multiple Clock Domain, Power-Aware, Tile-Based Embedded Processor

March 2004 **ACM SIGARCH Computer Architecture News , Proceedings of the 31st annual international symposium on Computer architecture**, Volume 32 Issue 2

Full text available: pdf(286.10 KB) Additional Information: full citation, abstract

We present Synchroscalar, a tile-based architecture forembedded processing that is designed to provide the flexibilityof DSPs while approaching the power efficiency ofASICs. We achieve this goal by providing high parallelismand voltage scaling while minimizing control and communicationcosts. Specifically, Synchroscalar uses columnsof processor tiles organized into statically-assignedfrequency-voltage domains to minimize power consumption.Furthermore, while columns use SIMD control to minimizeove ...

14 Regular contributions: DSP architectures: past, present and futures

Edwin J. Tan, Wendi B. Heinzelman

June 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 3

Full text available: pdf(1.27 MB) Additional Information: full citation, abstract, references

As far as the future of communication is concerned, we have seen that there is great demand for audio and video data to complement text. Digital signal processing (DSP) is the science that enables traditionally analog audio and video signals to be processed digitally for transmission, storage, reproduction and manipulation. In this paper, we will explain the various DSP architectures and its silicon implementation. We will also discuss the state-of-the art and examine the issues pertaining to pe ...

15 Session 7: embedded system techniques (2): Low Power Control Techniques For TFT LCD Displays

Franco Gatti, Andrea Acquaviva, Luca Benini, Bruno Ricco'

October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**

Full text available: pdf(314.45 KB) Additional Information: full citation, abstract, references, citings

Display power consumption is often the most significant contributor to the overall power budget for many portable devices. Traditionally, liquid crystal display (LCD) power minimization has focused on technology and circuit design. In this paper we take an orthogonal approach, and we introduce several software-only techniques for LCD dynamic power management, which do not require any hardware changes on existing LCDs and their controllers. The power savings achieved are significant: from 40% (wi ...

Results 1 - 15 of 15

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L1	4563	((341/131,144,155.110) or (375/22,254) or (370/292,276, 286) or (379/442,399.01)).CCLS.	USPAT	OR	OFF	2005/03/17 10:24
L2	0	codec transcoder dac adc	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/03/17 10:24
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L5	13	codec transcoder adc	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/03/17 10:25
L6	257	codec transcoder	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/03/17 10:25
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L9	0	codec transcoder dither	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/03/17 10:25
L10	12	codec adc dither	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/03/17 10:26
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L12	0	codec adc dither	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/03/17 10:26
L13	0	transcoder dac adc dither	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/03/17 10:27
L14	0	transcoder dac adc dither	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/03/17 10:27
L15	0	transcoder dac dither	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/03/17 10:27
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